OVER-60-GHz OPERATION OF SCFL DYNAMIC FREQUENCY DIVIDER USING InP-BASED HEMTs

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ABSTRACT

A toggle operation of 39 to 63.5 GHz has been achieved by a digital dynamic frequency divider. The frequency divider employes a pair of clocked inverters with source coupled FET logic (SCFL) and uses 0.1-μm-gate InAlAs/InGaAs/InP HEMTs with high uniformity and performance. On a 2-in. wafer the frequency divider showed a maximum toggle frequency of 59.1±3.3 GHz with a fabrication yield of 89%. This is the highest operation frequency yet obtained by a broadband digital frequency divider.

INTRODUCTION

InAlAs/InGaAs/InP HEMTs have demonstrated excellent ultrahigh-frequency [1], [2] and low-noise [3] performance and have been applied to various MMICs for the millimeter-wave band, such as low-noise amplifiers [4], [5], high-power amplifiers [6], traveling-wave amplifiers [7], mixers [8], oscillators [9], and the integration of these kinds of analogue circuits [10]. In contrast with microwave circuit applications, few applications have been made in digital ICs, i.e., the 26.7-GHz frequency divider [11], because of the greater difficulty of attaining larger-scale integration in digital ICs than in MMICs. Using a T-shaped gate and an InP recess-etch stopper in these types of HEMTs and using source coupled FET logic (SCFL) gates [12], we have been able to make a 40.4-GHz static frequency divider [13], a 46-Gbit/s multiplexer [14], and a 40-Gbit/s demultiplexer [14] for optical transmission systems. For emerging frequency-division applications in the frequency range far above 40 GHz, however, dynamic frequency dividers (DFD) are the only demonstrated solution. Two types of analog DFDs have been recently reported: a 57 to 64-GHz regenerative DFD IC using GaAs-based HEMTs [15] and a 75-GHz DFD IC with an injection-locked push-pull oscillator using the same type of InP-based HEMTs [16]. These types of DFDs are advantageous in ultra-fast operation, however, their locking range for a fixed bias condition is intrinsically narrow. Therefore, these types of DFDs need tuning to operate for a broad frequency range, as presented in Ref. 16. Digital frequency dividers in contrast have a broadband operation range without tuning as well as high-speed operation. For example, a report has been made on a 28-51 GHz DFD IC with dual ring oscillators gated by transfer gates using GaAs-based HEMTs [17], and a 25-50 GHz DFD IC with a dynamic toggle flip-flop (T-FF) composed of two clocked inverters using GaAs-based HBTs [18]. We adopted the latter type of digital DFDs because the basic gate of this type of frequency divider is the same as the one for digital circuits such as the dynamic D flip-flop (D-FF) [19]. Therefore, this type of frequency divider can also be used as a bench mark for the maximum operation frequency of ultrahigh-speed digital ICs in dynamic operation.

In this paper we describe the design and performance of a DFD with a pair of SCFL clocked inverters using InAlAs/InGaAs/InP HEMTs. The advantage of clocked inverters in broadband operation and the high uniformity and performance of the HEMTs give this frequency divider 63.5-GHz toggle operation and a 24.5-GHz operation bandwidth

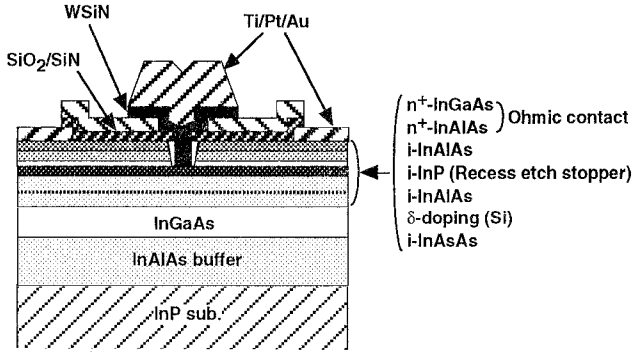

Fig. 1. Structure of an InAlAs/InGaAs/InP HEMT with a T-shaped gate, WSiN refractory gate metal, an SiO_2/SiN bilayer dielectric-film system, and an InP recess-etch stopper.

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without tuning. This frequency divider demonstrates the feasibility of digital circuits operating over 60 GHz.

InAlAs/InGaAs/InP HEMT

Figure 1 shows a cross section of the HEMT, which has a gate length of 0.1 μm. An InAlAs/InGaAs modulation-doped heterostructure lattice-matched to InP substrate was grown by MOCVD. A direct EB writer and conventional optical lithography were respectively used to delineate the footprint and the top part of the T-shaped-gate electrode [20] with high accuracy and reproducibility in size. WSiN was used as the Schottky-contact metal to improve thermal hardness [21]. A SiO_2/SiN bilayer dielectric-film system [22] on the semiconductor surface was used to reduce the aspect ratio of the narrow groove for the gate footprint and to completely fill the groove with WSiN. To ensure the uniformity of the gate-recess depth an InP layer was inserted into the InAlAs barrier layer as a gate-recess-etch stopper [20]. Figure 2 shows the distribution of threshold voltage (V_{th}) and transconductance (g_m) for the HEMTs on a 2-in. wafer on which the frequency dividers were fabricated. By using an InP recess-etch stopper, the standard deviation (σ) of V_{th} was reduced to only 25 mV. Moreover, the g_m of these HEMTs is 890±36 mS/mm (mean±σ). The current-gain cutoff frequency (f_T) of the HEMTs was high and uniform: 164±7.6 GHz. Seventy-one of 72 FETs on the 2-in. wafer worked well.

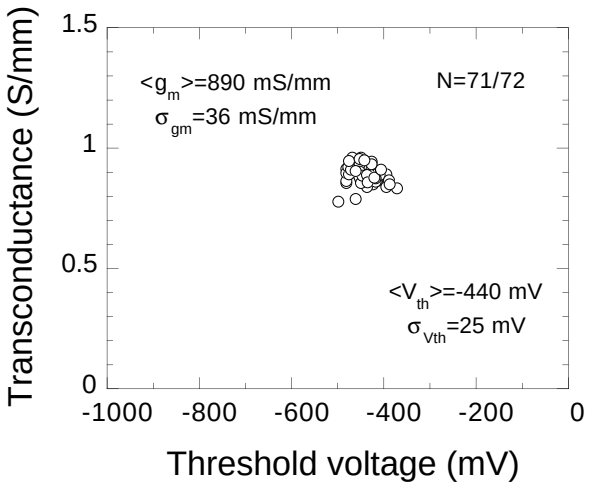

Fig. 2. Transconductance (g_m) versus threshold voltage (V_{th}) for 0.1-μm-gate HEMTs on a 2-inch wafer.

FREQUENCY DIVIDER

Ultrahigh-speed broadband frequency dividers using a dynamic T-FF composed of two clocked inverters (Fig. 3) were fabricated using the InAlAs/InGaAs/InP HEMTs described above. The frequency divider consisted of an input buffer converting a single-ended input signal to a differential signal, a dynamic T-FF, and an output buffer driving 50-Ω lines. To ensure high-speed operation, we minimized the signal path length in order to reduce the signal transit delay through interconnection lines [23]. As a result, the critical signal path for a clocked inverter was around 300 μm, resulting in a delay of 2.6 ps/gate. This is reasonably small when compared with the total delay of 8.3 ps/gate for a clocked inverter operating at 60 GHz. In addition, the

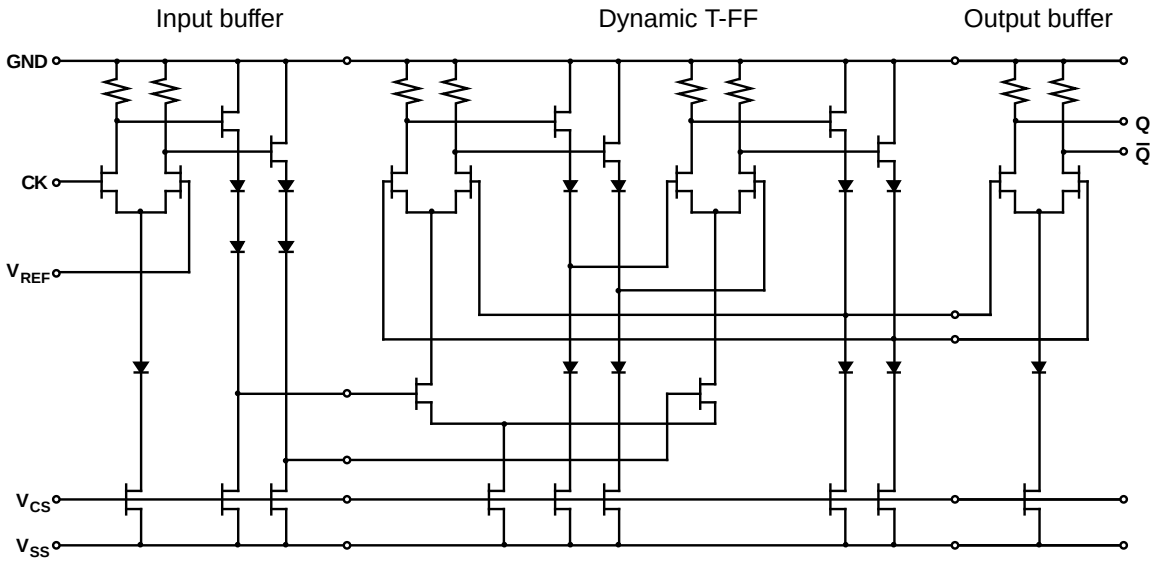

Fig. 3. Circuit diagram of the SCFL dynamic frequency divider using dynamic T-FF composed of two clocked inverters.

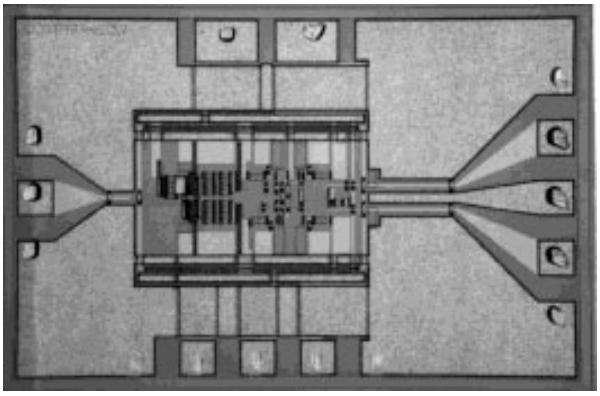

Fig. 4. Photomicrograph of a dynamic frequency divider using 0.1-μm InAlAs/InGaAs/InP HEMTs.

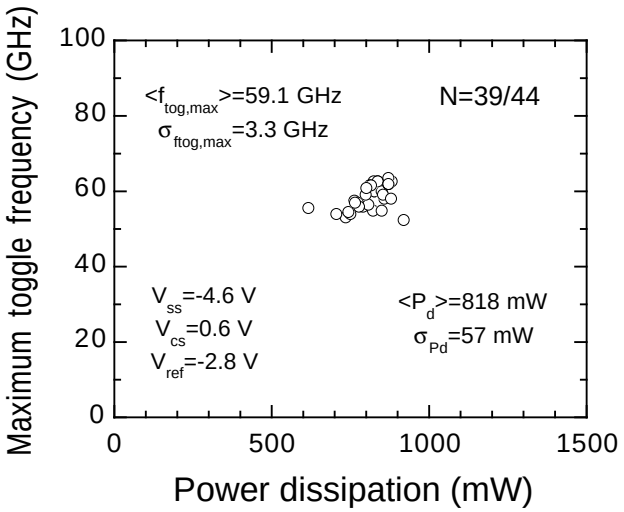

Fig. 5. Scatter plot of maximum toggle frequency (f_{togmax}) and power dissipation (P_d) of dynamic frequency dividers on a 2-in. wafer.

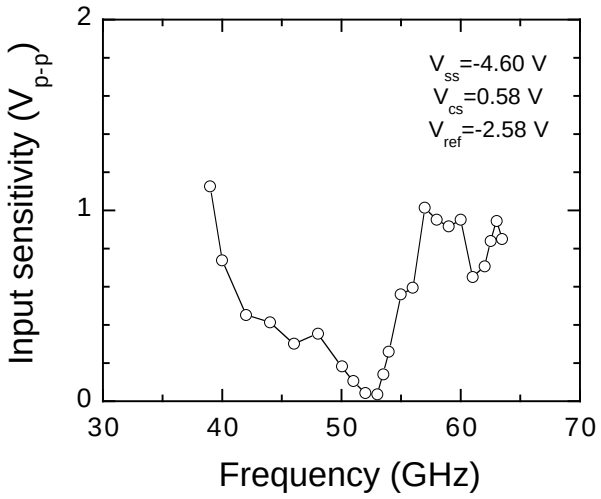

Fig. 6. Input sensitivity versus frequency of a frequency divider. The frequency of self-oscillation is 52.5 GHz.

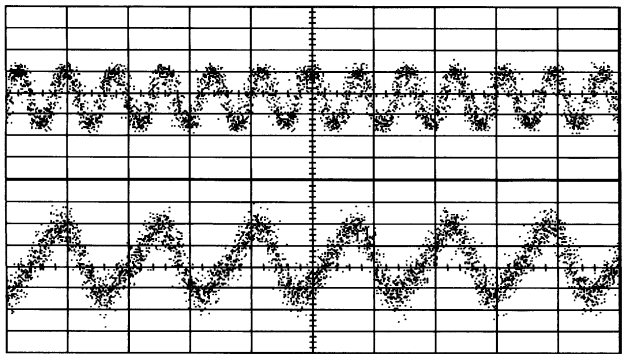

Fig. 7. Input and output waveforms of a frequency divider. The input (upper) and the output (lower) frequencies are respectively 63.5 and 31.75 GHz and their amplitudes are 850 and 140 mV.

output impedances of each stage of the clocked inverters are matched as closely as possible to the ones of the interconnection lines by optimizing the gate width of the FETs [23]. The optimised gate width for the FETs in the T-FF was 20 μm. The gate width for the input buffer was chosen to be 50 μm so as to give priority to driving capability, whereas a 20-μm gate width were used for the output buffer to make the buffer compatible with sufficient output amplitude and a small enough degradation in speed. Figure 4 is a photomicrograph of the frequency divider, whose chip size is 1.4 x 0.9 mm. Figure 5 shows the distribution of the maximum toggle frequency (f_{togmax}) and the power dissipation (P_d) of the frequency dividers on a 2-in. wafer. The fabrication yield for 44 samples was 89% and the f_{togmax} was 59.1±3.3 GHz. Figure 6 shows an input sensitivity for one of these frequency dividers, which showed stable toggle operation up to 63.5 GHz. The operation bandwidth is as broad as 24.5 GHz without tuning. Figure 7 shows an input and output waveform of the frequency divider at 63.5 GHz. To our knowledge, this operation frequency is the highest for any digital frequency dividers.

CONCLUSION

Digital dynamic frequency dividers employing SCFL clocked inverters were fabricated using 0.1-μm InAlAs/InGaAs/InP HEMTs with high uniformity and performance. A frequency divider achieved record toggle operation at 38 to 63.5 GHz without tuning. Moreover, they showed excellent yield and uniformity: a fabrication yield of 89% and a f_{togmax} of 59.1±3.3 GHz on a 2-in. wafer. These results show that high-speed ICs which can operate at over 60 Gbit/s will be achievable by using these technologies.

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